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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,006	ANDERSON ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/13/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11 June 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it is directed to the method, which was restricted and not elected for this application. Applicant should submit a new abstract directed to the structure that is the subject of the elected claims.

Claim Objections

2. Claims 9, 10, and 14 are objected to because of the following informalities: the recitation "source/drain" is inappropriate. The slash could be interpreted multiple ways, applicant should spell out whether "and" or "or" or "and/or" is meant by the slash. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4-6 and 12-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 4 contains the recitation "...wherein said transistor comprises a CMOS..." A CMOS device, by definition, comprises at least two transistors. Therefore, a single transistor cannot comprise a CMOS device. Perhaps applicant means "...wherein said transistor is one of a plurality of transistors comprised by a CMOS..."

6. Claim 5 contains the recitations "nFET configuration" and "pFET configuration". It is unclear exactly what the metes and bounds of these limitations are. Applicant should clearly define what structure comprises the claimed "configuration".

7. Claim 6 contains the recitation "...ion implantation levels for each of said nFET configuration and said pFET configuration..." It is unclear which components of said configurations are being referred to. For example, this may refer to the ion implantation levels of drain dopants. Applicant should clearly define what is being implanted, and into which structure it is being implanted.

8. Claim 12 contains the recitations "nFET region" and "pFET region". It is unclear exactly what the metes and bounds of these limitations are. Applicant should clearly define what structure comprises the claimed "region".

9. Claim 13 contains the recitation "...ion implantation levels for each of said nFET region and pFET region..." It is unclear which components of said regions are being referred to. For example, this may refer to the ion implantation levels of drain dopants. Applicant should clearly define what is being implanted, and into which structure it is being implanted.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 2004/0195628), hereinafter Wu, in view of McCaldin et al. (US 3,328,210), hereinafter McCaldin.

12. Regarding claim 1, Wu discloses (FIG. 5B) a field effect transistor (5,6; [0015] ln 1-2) (FET) comprising:

a source (FIGS 9A-10 ref 30 and 40; [0023] ln 8-10) region;

a drain (FIGS 9A-10 ref 30 and 40; [0023] ln 8-10) region;

a channel (FIGS 5B & 9A, area under gate 8 between source and drain is a channel) region disposed between the source and drain regions;

a bifurcated gate (8; [0018] ln 12-13; dictionary defines bifurcated as forked) region positioned over said channel region; and

a gate oxide layer (7; [0017] ln 5) adjacent to said gate region, but does not disclose, "wherein said gate oxide layer comprises an alkali metal ion." McCaldin is directed toward the same field of endeavor, field effect transistors with decreased channel resistance. McCaldin teaches (Fig. 2) the use of alkali metal ions in the gate oxide (25; col 1 ln 26-27; col 2 ln 51-55).

13. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the field effect transistor of Wu by including an alkali metal ion in the gate oxide, as taught by McCaldin; for at least the purpose of increasing channel conductance (col 4 ln 30-33).

14. Regarding claim 2, Wu discloses (FIG. 5B) the transistor of claim 1, further comprising:

a substrate (1; [0015] ln 9);

an isolation layer (2; [0015] ln 10) positioned over said substrate;

and at least one fin structure (3 in transistors 5 & 6; [0016] ln 3) disposed between the source and drain regions (FIG. 9A: 30 & 40; [0023] ln 12-15);

wherein said source and drain regions are positioned over said isolation layer (FIG. 10 clearly shows source/drains 30 & 40 positioned over isolation 2).

15. Regarding claim 3, Wu discloses the transistor of claim 1, but does not disclose, "wherein said alkali metal ion comprises any of cesium and rubidium." However, McCaldin teaches the use of the alkali metal ions cesium and rubidium (col 1 ln 34-35).

16. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use either Cesium or Rubidium for the alkali metal ions, as taught by McCaldin; for at least the purpose of increasing channel conductance by inducing a negative charge in the channel region (McCaldin col 2 ln 57-59). Further, since it is known in materials science that Cesium and Rubidium are extremely electropositive, they are obvious choices for positive ions.

17. Regarding claim 4, Wu discloses (FIG. 5B) the transistor of claim 1, wherein said transistor comprises a CMOS (complimentary metal oxide semiconductor) device (nMOS/pMOS 5/6; [0023] ln 12-15).

18. Regarding claim 5, Wu discloses (FIG. 5B) the transistor of claim 4, wherein said CMOS device comprises any of a nFET (5) configuration and a pFET (6) configuration ([0023] ln 12-15).

19. Regarding claim 6, Wu discloses the transistor of claim 5, but does not disclose "further comprising ion-implantation levels for each of said nFET configuration and said pFET configuration of approximately 3 x 10^{18} cm^{-3}." McCaldin teaches the use of alkali metal ions (col 1 ln 26-27; col 2 ln 51-55), but does not teach the claimed implantation levels.

20. However, it would have been obvious to one having ordinary skill in the art at the time of the invention to use ion-implantation levels of approximately 3 x 10^{18} cm^{-3}, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

21. Regarding claim 7, Wu discloses (FIG. 5B) the transistor of claim 1, wherein said gate region comprises silicide (8; [0018] ln 2 & 12).

22. Regarding claim 8, Wu discloses the transistor of claim 5, but does not disclose "wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET configurations by an amount required to match desired off-currents for said nFET and PFET configurations." However, McCaldin teaches the use of alkali metal ions (col 1 ln 26-27; col 2 ln 51-55) for modifying electrical characteristics of a field effect transistor (col 4 ln 62-64).

23. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the nFET and pFET threshold voltages for the nFET and pFET configurations by an amount required to match desired off-currents for said nFET and PFET configurations; for at least the purpose of having a threshold voltage value appropriate to the particular chosen circuit design. Further, it has been held that

discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

24. Regarding claim 9, Wu discloses (FIG. 5B) a (field effect transistor) CMOS (complementary metal oxide semiconductor) device (nMOS/pMOS 5/6; [0023] ln 12-15) comprising:

raised source/drain regions (FIGS. 9A &10: 30 & 40; [0023] ln 12-15);

a channel region (FIGS 5B & 9A: area under gate 8 between source and drain is a channel) disposed between said source/drain regions;

a gate region (8; [0018] ln 12-13) positioned over said channel region;

a silicon layer (3; [0015] ln 7) dividing said gate region; and

a gate oxide layer (7; [0017] ln 5) adjacent to said gate region, but does not disclose "wherein said gate oxide layer comprises an alkali metal ion." McCaldin is directed toward the same field of endeavor, field effect transistors with decreased channel resistance. McCaldin teaches (Fig. 2) the use of alkali metal ions in the gate oxide (25; col 1 ln 26-27; col 2 ln 51-55).

25. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the field effect transistor of Wu by including an alkali metal ion in the gate oxide, as taught by McCaldin; for at least the purpose of increasing channel conductance (col 4 ln 30-33).

26. Regarding claim 10, Wu discloses (FIG. 5B) the device of claim 9, further comprising:

a substrate (1; [0015] ln 9) ;

an isolation layer (2; [0015] ln 10) positioned over said substrate; and

at least one fin structure (3 in transistors 5 & 6; [0016] ln 3) disposed between the source and drain regions (FIG. 9A: 30 & 40; [0023] ln 12-15);

wherein said source/drain regions are positioned over said isolation layer (FIG. 10 clearly shows source/drains 30 & 40 positioned over isolation 2).

27. Regarding claim 11, Wu discloses the device of claim 9, but does not disclose, "wherein said alkali metal ion comprises any of cesium and rubidium." However, McCaldin teaches the use of the alkali metal ions cesium and rubidium (col 1 ln 34-35).

28. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to use either Cesium or Rubidium for the alkali metal ions, as taught by McCaldin; for at least the purpose of increasing channel conductance by inducing a negative charge in the channel region (McCaldin col 2 ln 57-59). Further, since it is known in materials science that Cesium and Rubidium are extremely electropositive, they are obvious choices for positive ions.

29. Regarding claim 12, Wu discloses (FIG. 5B) the device of claim 9, further comprising any of a nFET (5) region and a pFET (6) region ([0023] ln 12-15).

30. Regarding claim 13, Wu discloses the device of claim 12, but does not disclose "further comprising ion-implantation levels for each of said nFET configuration and said pFET configuration of approximately 3×10^{18} cm^{-3}." McCaldin teaches the use of alkali metal ions (col 1 ln 26-27; col 2 ln 51-55), but does not teach the claimed implantation levels.

31. However, it would have been obvious to one having ordinary skill in the art at the time of the invention to use ion-implantation levels of approximately 3×10^{18} cm^{-3}, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

32. Regarding claim 14, Wu discloses (FIG. 5B) the device of claim 9, further comprising spacers (9; [0020] ln 1) separating said gate region from said source/drain regions.

33. Regarding claim 15, Wu discloses the device of claim 9, wherein said gate region comprises silicide (8; [0018] ln 2 & 12).

34. Regarding claim 16, Wu discloses the device of claim 12, but does not disclose "wherein said alkali metal ion adjusts nFET and pFET threshold voltages for the nFET and pFET regions by an amount required to match desired off-currents for said nFET and PFET regions." However, McCaldin teaches the use of alkali metal ions (col 1 ln 26-27; col 2 ln 51-55) for modifying electrical characteristics of a field effect transistor (col 4 ln 62-64).

35. Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to adjust the nFET and pFET threshold voltages for the nFET and pFET regions by an amount required to match desired off-currents for said nFET and PFET regions; for at least the purpose of having a threshold voltage value appropriate to the particular chosen circuit design. Further, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven Loke
Primary Examiner